App. No. 10/727,676
Office Action Dated September 7, 2005

Amendments to the Specification

Please amend the paragraphs on page 1, line 28 to page 2, line 11 as follows:

The solid-state imaging device 90 includes a vertical driving circuit 12. A plurality of reset transistor control lines 111 are connected to the vertical driving circuit 12. The reset transistor control lines 111 are arranged at a predetermined distance from and parallel to each other along a horizontal direction so as to be connected respectively to the reset transistors 15 that are provided respectively in the pixel cells 96 laid out along the horizontal direction. A plurality of vertical select transistor control lines 121 further are connected to the vertical driving circuit 12. The vertical select transistor control lines 121 are arranged at a predetermined distance from and parallel to each other along the horizontal direction so as to be connected respectively to vertical select transistors 16 that are provided respectively in the pixel cells 96 laid out along the horizontal direction. The vertical select transistor control lines 121 determine from which row signals are to be read out.

The respective sources of the vertical select transistors 16 are connected to vertical signal lines 61. A load transistor group 17 is connected to one end of each of the vertical signal lines 61. The other end of each of the vertical signal lines 61 is connected to a row signal storing part 18. The row signal storing part 18 includes a switching transistor for capturing signals to be obtained from one row. A horizontal driving circuit 13 is connected to the row signal storing part 18.

Please amend the paragraph on page 2, lines 14-18 as follows:

When a row selection pulse 101−1 for increasing the power level of the vertical select transistor control line 121 is applied, the vertical select transistors 16 in a selected row are activated, so that the amplify transistors 14 in the selected row and the load transistor group 17 form a source follower circuit.

Please amend the paragraph on page 11, lines 3-7 as follows:

As described above, by covering the STI stress defect layer 95 with the STI leakage stopper 1, as shown in FIG. 6, a pn junction reverse-direction leakage current that is generated from around the element isolating portion 2 can be suppressed. Thus, a high-performance MOS type solid-state imaging device can be realized. In Fig. 6, numeral 88 denotes a STI stress defect layer.